IP-DDC

v1.0

Innovative Integration
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Single Channel Digital Downconversion Core for FPGA

FEATURES

- Single channel 24 bit DDC
- 16 bit input @ Max 250 MSPS
- Tuning resolution up to 0.0582 Hz
- SFDR >115 dB for 16 bits input
- DDC decimation range from 2 to 32768
- Programmable 20 tap CFIR (18 bit)
- Programmable 80 tap PFIR (18 bit)
- Embedded spectrum inversion
- Bypass decimation filters capability
- DDC gain control up to 60 dB gain
- DDC overflow indicator
- Embedded power meter (-77dBm ~ 13dBm)
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Digital Receivers
- Image Processing
- Spectrum Analysis

HARDWARE SUPPORT

- Support Xilinx Virtex-6, Virtex-5 FPGA
- Innovative X5 and X6 family of XMC Modules

DELIVERABLES

- Netlist or MATLAB/Simulink source code
- MATLAB/Simulink simulation model with test vectors
- Implementation control files for Innovative X5/X6 family
- User manual and application notes

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Description

The IP-DDC core has single output channel of digital down-conversion (DDC). As a flexible front-end to receivers and imaging devices, this core implements the frequency translation for baseband signal recovery as FPGA firmware.

The DDC has programmable tuning frequency, filtering, gain control, and decimation setting, supporting output bandwidth up to 125 MHz when the input data rate is 250 MSPS. The DDC channel tunes to a band through a programmable 32-bit tuner that ranges from DC to Fs/2, where Fs is the A/D sampling frequency. The decimation filters are composed of a CIC compiler, a compensation filter (CFIR), and a programmable filter (PFIR). The CIC compiler is programmable to provide a decimation rate from 4 to 8192, while the CFIR and PFIR are both decimation by 2 filters. This gives a total decimation of 2 to 32768 for the channel with the bypass capability of each filter. The channel rejection is up to 90dB, and the SFDR is over 115 dB for the 16 bit inputs. Gain adjustment is allowed after each decimation filter, and an overflow indicator is provided to prevent arithmetic overflow. A power meter is attached to the DDC input and output data, which allows the user to monitor both the wideband input power and the narrowband output power.

The core is targeted at the Xilinx Virtex5 SX95T FPGA and consumes about 23% of an SX95T device. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

Simulation models for system design are provided as fixed point MATLAB/Simulink files. The model is bit-true, cycle-true for device simulation. Source is available for purchase.

04/01/11

IP-DDC

Ordering Information

Product	Part Number	Description
IP-DDC	58021-0	Netlist version bundled with X6/X5 boards
	58021-1	Netlist Version Only
	58021-2	Source Code Version

Table 1. Product information

Block Diagram

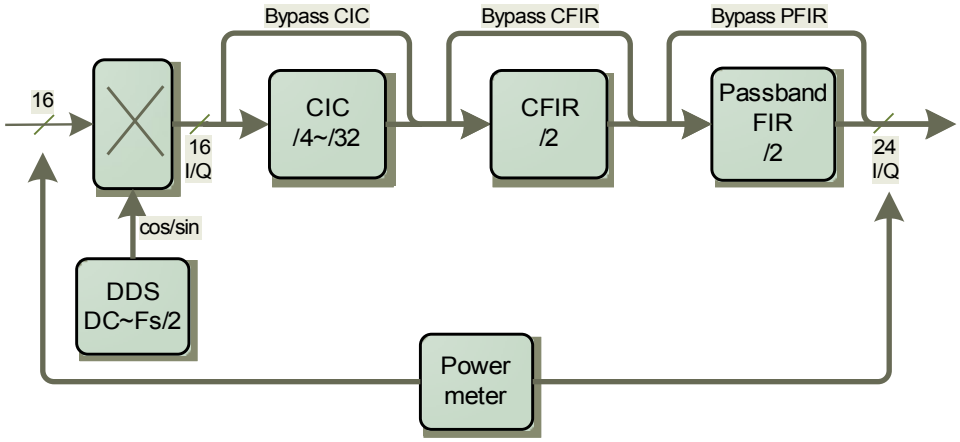


Figure 1. IP-DDC block diagram

Figure 1 shows the DDC structure utilizing the tuner and the decimation filters. Bypass path provides the capability to deal with high bandwidth signal by using different combination of filters.

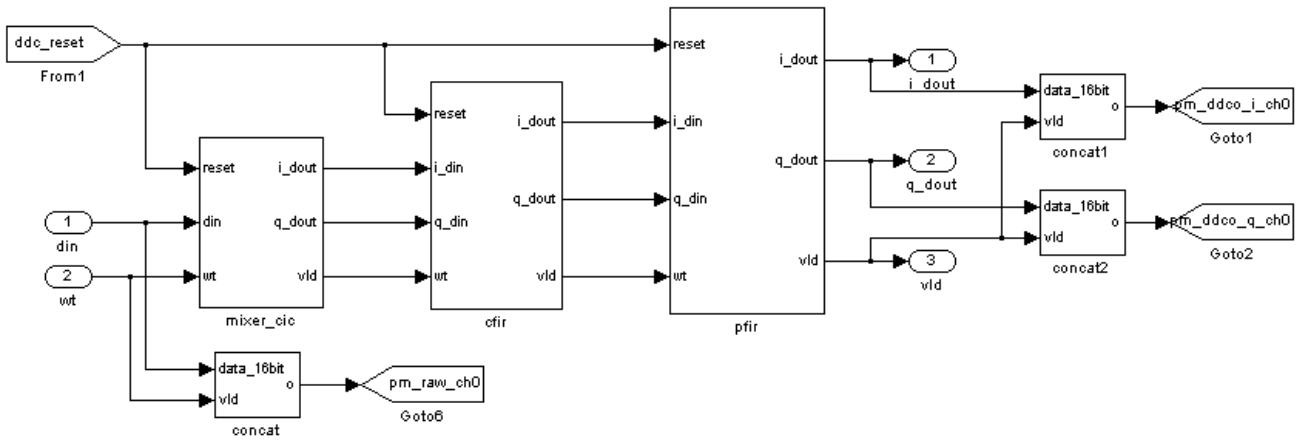


Figure 2. MATLAB/Simulink project of IP-DDC

Figure 2 shows the DDC built under MATLAB/Simulink environment using Xilinx System Generator blockset. All the signal processing blocks utilize cores from Xilinx System Generator and guaranteed to be bit true and cycle true as in the FPGA hardware. In Figure 3, the core is integrated with the analog frontend and FrameWork logic components for the Software Defined Radio (SDR) project on X5-210M. This system is built on the COTS (Commercial Off-The-Shelf) product, providing high performance and full upgrades to the next generation hardware using the same IP core.

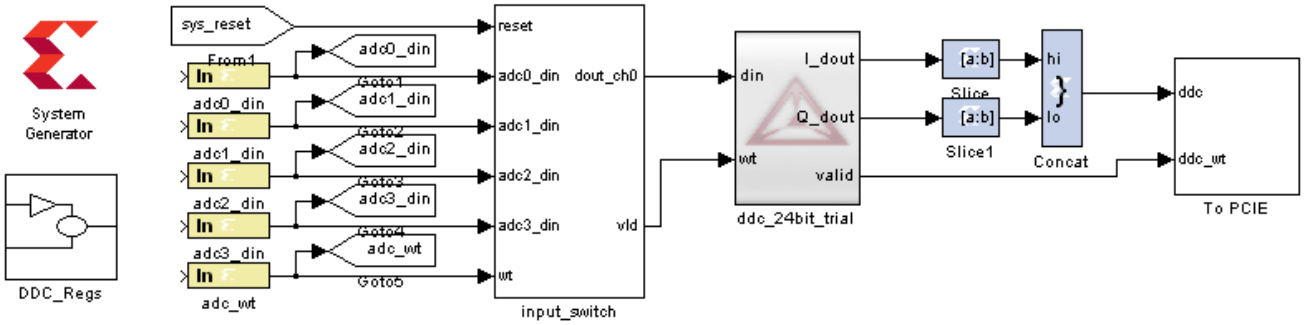


Figure 3. MATLAB/Simulink system integration of IP-DDC on X5-210M

IP-DDC

Port Description

Signal	Size	Direction	Description
clk_1	1	In	Clock
ce_1	1	In	Clock enable; set to '1'.
ddc_reset	1	In	Asynchronous reset for DDC core
ddc_din	16	In	16 bit input data
ddc_wt	1	In	Input data write strobe
tune_freq_word	32	In	Tuning frequency for the tuner
tune_freq_wt	1	In	Tuning frequency write strobe
delta_word	24	In	Delta frequency for fine tune
delta_wt	1	In	Delta frequency write strobe
cic_rate	14	In	CIC filter decimation rate
cic_rate_wt	1	In	CIC rate write strobe
cfir_coef	18	In	Compensation filter (CFIR) coefficient input
cfir_coef_wt	1	In	CFIR coefficient write strobe
pfir_coef	18	In	Programmable filter (PFIR) coefficient input
pfir_coef_wt	1	In	PFIR coefficient write strobe
cic_rate	14	In	CIC filter decimation rate; range from 4 ~ 8192
cic_rate_wt	1	In	CIC rate write strobe
cic_bstart	8	In	CIC filter outputs gain control, which specify the starting bit of the LSB.
cic_bstart_wt	1	In	CIC bstart write strobe
cfir_bstart	7	In	CFIR outputs gain control, which specify the starting bit of the LSB.
pfir_bstart	7	In	PFIR outputs gain control, which specify the starting bit of the LSB.
fir_bstart_wt	1	In	CFIR, PFIR bstart write strobe
spect_inv	1	In	Spectrum inversion enable
bp_cic	1	In	Bypass CIC filter
bp_cfir	1	In	Bypass CFIR
bp_pfir	1	In	Bypass PFIR
ddc_ovflo_rd	1	In	DDC CIC, CFIR, PFIR overflow read strobe
pmeter_acc_pts	5	In	Power meter accumulate points
pmeter_src_sel	12	In	Power meter source select
ddc_i_dout	24	Out	DDC I output
ddc_q_dout	24	Out	DDC Q output
ddc_vld	1	Out	DDC output valid
ddc_ovflo	3	Out	DDC overflow signal
ddc_ovflo_alert	1	Out	DDC overflow alert
pmeter_dout	32	Out	Power meter data

Table 2. I/O port table

IP-DDC

Example Implementation

This example shows the GSM receiver implementation of IP-DDC on Innovative X5-210M board.

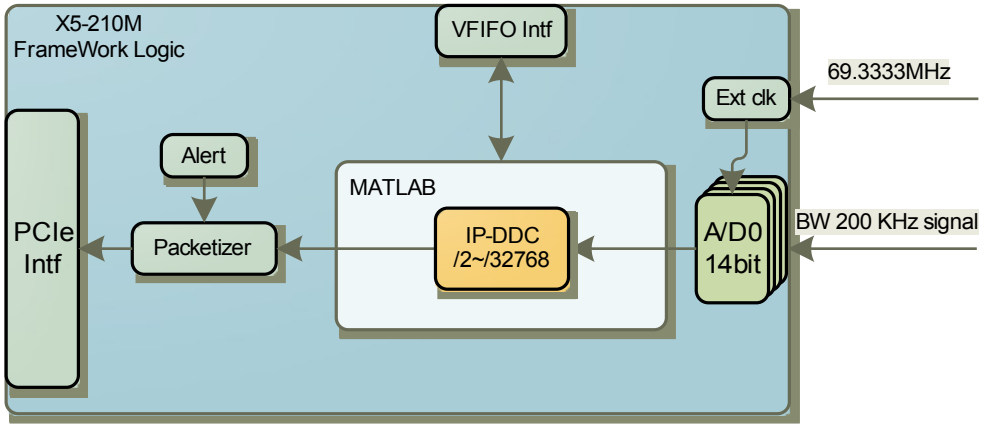
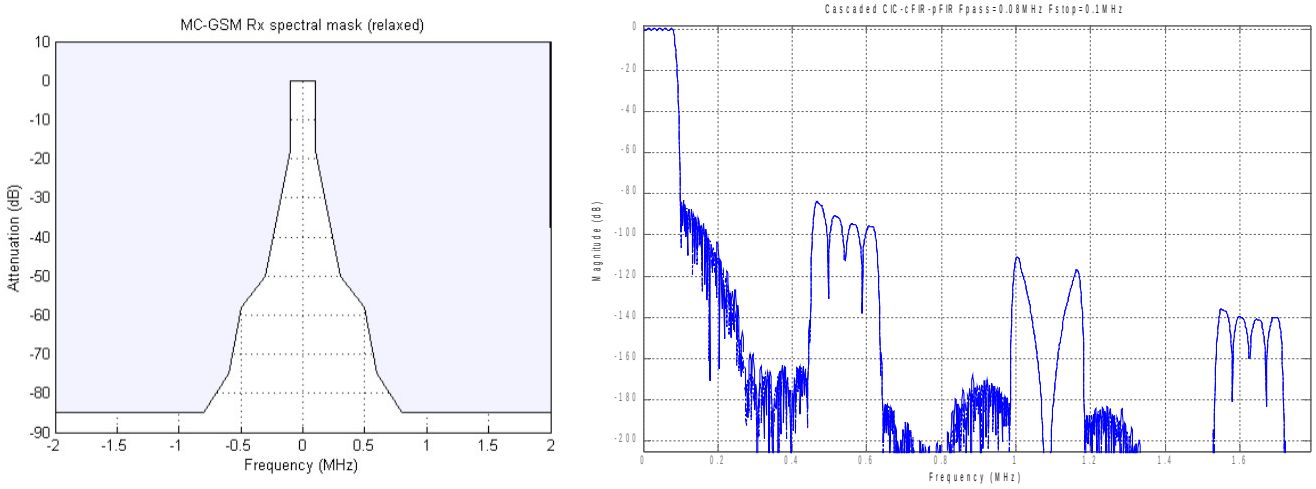


Figure 4. GSM DDC receiver using IP-DDC on X5-210M

Parameter	Value
Channel Bandwidth	200 KHz
Baseband Symbol Rate	270.8333 KSPS
IF Sample Rate	69.3333 MSPS
SFDR	Up to 115 dB

Table 3. GSM receiver specification



(a) (b)

Figure 5. (a) Desired GSM spectral mask, see [Ref 1]; (b) designed DDC frequency response.

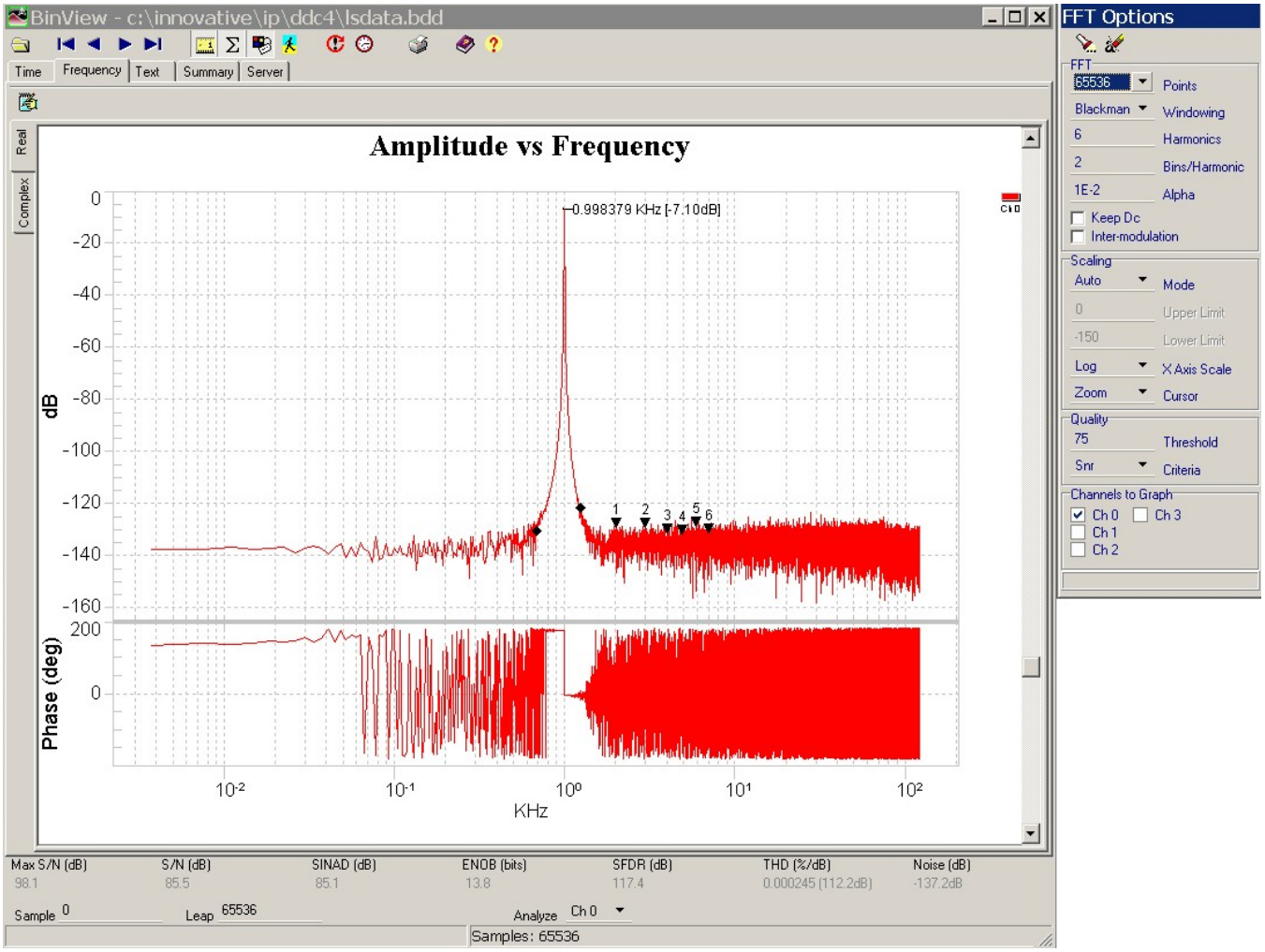


Figure 6. Typical core performance

IP-DDC

Standard Features

Inputs	
Input Ch. Num.	1
Input Format	16-bit, 2's complement, real
Input Rate	250 MHz maximum @ 250 MHz clock *
Outputs	
Output Ch. Num.	1
Output Format	24-bit, 2's complement, I/Q
Output Rate	Fs/2 to Fs/32768
Channel Tuning	
Tuning Range	DC to Fs/2
Tuning Resolution	Fs/2^32
CIC Filter	
Stage	4
Differential Delay	2
Decimation Rate	4 to 8192; programmable
Compensation Filter	
Taps	20; programmable
Taps Resolution	18 bit
Programmable Filter	
Taps	80; programmable
Taps Resolution	18 bit
Other	
Bypass Filters	Available for CIC, CFIR, PFIR
Spectral Inversion	Available
Gain Range	0 to 60 dB
Overflow Indicator	Available after each filter
Power Meter	Available for DDC input/outputs

* Note: Higher input sample rate can be achieved by increasing the clock of the core.

Performance	
SFDR	> 115 dB (16 bit input)
S/N	Up to 90 dB

Device Utilization		
Element	FPGA Resource	Virtex-5 SX95T
FF	13553	23%
LUT	8286	14%
DSP48E	122	19%
BlockRAM	52	21%

Reference

1. Creaney S. & Kostarnov, I. (2008). *Designing Efficient Digital Up and Down Converters for Narrowband Systems*. Retrieved from Xilinx, Inc. Xilinx, Inc website: http://www.xilinx.com/support/documentation/application_notes/xapp1113.pdf

IP-DDC

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