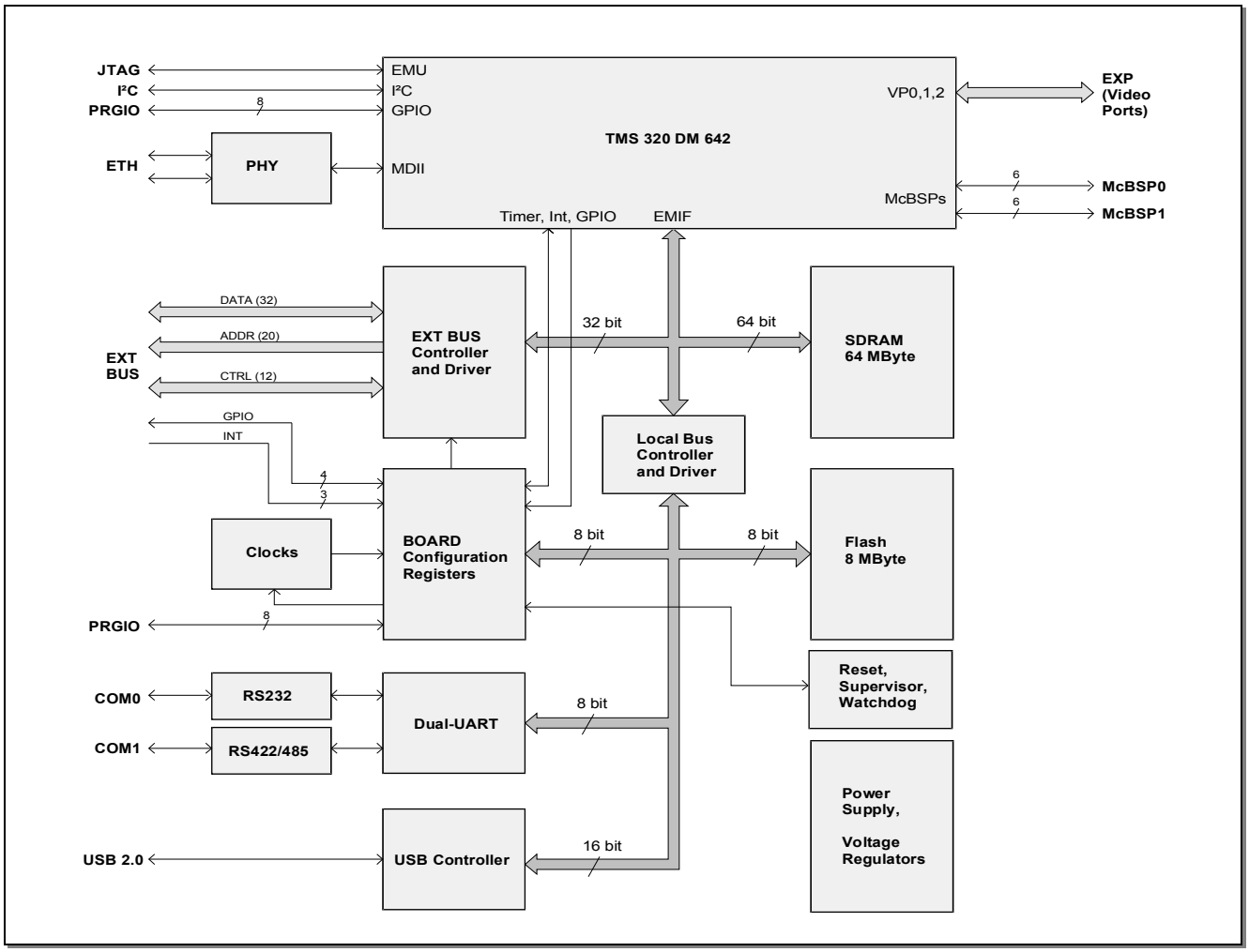
D.Module2.DM642 Technical Data Sheet

Board Revision 1.1 **Document Rev. 1.2** **Nov/2014**

SUMMARY

- **High performance fixed-point DSP module for video and image processing, radar, sonar, ultrasonics, and biometrics**
- **5760 MIPS Texas Instruments TMS320DM642 DSP**
- **Three 80 MHz buffered video ports for cameras, video-interfaces, and high-speed ADCs and DACs**
- **533 Mbytes/s external bus bandwidth**
- **Large on-board memories: 64M-Byte SDRAM, 8M-Byte non-volatile Flash**
- **10Base-T / 100Base-TX Ethernet controller**
- **High-speed USB2.0 peripheral controller**
- **Dual-UART with auto-flow control, receive and transmit FIFOs, RS232 and RS422/485 interface**
- **3.3V single-supply, Supervisor and Watchdog**
- **D.Module2.BIOS programming support for all on-board resources, USB / RS232-based Setup Utility for convenient field-maintenance**

BLOCK DIAGRAM



The D.Module2 series represents the next generation of high-performance,stand-alone DSP boards. These boards are optimized for highest I/O bandwidth to satisfy even demanding applications. The 32-bit wide external bus, configured in synchronous mode, can transfer up to 533 Mbytes/s of data between DSP and peripherals.

The self-stacking design allows to build complete signal processing systems by stacking the required DSP, I/O, data acquisition,and networking modules. If data preprocessing is needed an FPGA module can be inserted between data acquisition and DSP.

Besides the high-speed peripheral bus all D.Module2 DSP boards provide a variety of interfaces: two UARTs, an USB2.0 peripheral controller, user-programmable I/O ports, and synchronous serial interfaces. An extra connector is reserved for DSP-specific extensions like the video ports in case of the DM642 module.

The high-speed design required special care for signal integrity and EMC. The PCB uses auxiliary GND planes to shield signals and provide controlled impedance signal paths, the power supply lines are extensively filtered, and the connector pinout provides ample signal return ground connections.

Programming support for all on-board peripherals is provided by the D.Module2.BIOS, a set of functions resident in the module's Flash Memory, covering initialization, configuration, and data transfer. Hardware dependencies are encapsulated by the BIOS, hence no software adaptations due to peripheral component or silicon revision changes are required in the user and application programs.

A Setup Utility, also resident in the Flash Memory, provides straightforward field maintenance via USB or RS232: data and program upload, configuration changes, and basic debugging functionality are available without the need for special emulator or programming equipment.

PROCESSOR

The DModule2.DM642 is built around the Texas Instruments TMS320DM642 fixed-point DSP. The TMS320C64x™ core provides 64 32-bit general purpose registers, six ALUs, and two multipliers. The ALUs support single 32-bit, double 16-bit, or quad 8-bit operations per cycle, making this DSP an excellent choice for image processing and related algorithms.

The DM642 also features three built-in video ports with capture and display buffers. These ports allow glueless connection to most image sensors, video encoders and decoders, and high-speed A/D and D/A converters.

SDRAM

64 Mbytes, 64-bit wide SDRAM is used on the D.Module2.DM642. Operating at up to 133 MHz, a throughput of 1 Gbyte/s can be achieved. SDRAM can be used for program code and data. The advanced L1 and 4-way L2 caches of the DM642 further optimize memory performance.

FLASH MEMORY

8 Mbytes non-volatile Flash Memory provide storage for application programs, user data, and configuration settings. The Flash Memory also stores the board's hardware settings, the D.Module2.BIOS API functions, and the Setup and Recovery Utility programs. The D.Module2.BIOS functions provide erase, (block)write and (block)read functions, and a function to program the Flash with Intel-Hex files. The bootload function loads and executes programs stored in the Flash Memory.

Two boot sectors are hardware write protected. These sectors hold the module hardware configuration and the Recovery utility program. Even in case the flash memory is completely erased or overwritten by accident, these sectors remain intact and allow to recover the D.Module2.BIOS and the application without any special programming equipment.

EXTERNAL BUS INTERFACE

The bus interface is used to connect external peripherals like data acquisition boards or FPGAs.. It is configurable to asynchronous and synchronous mode. Synchronous mode, achieves data transfer rates up to 533 Mbytes/sec and supports FlyBy DMA transfers between SDRAM and external devices. Asynchronous transfer timing is widely programmable. External device can request additional wait states via the WAIT_N input. Up to 133 Mbytes/sec. throughput can be achieved.

The bus interface uses a 32 bit wide data bus, 12 control signals, 20 address lines, and three external interrupt or DMA request inputs. Four GPIO signals are configurable in the Board Configuration Register and allow to route DSP Timer and/or GPIO signals to external peripherals. Two predecoded memory areas are available, which can be individually configured to different data formats, synchronous or asynchronous operation, and bus timings.

The bus drivers source/sink up to 24mA and are able to drive long signal lines with passive or active termination. In synchronous configuration the bus drivers operate registered to maximize setup and hold timing margins for the external peripherals.

USB

The Philips isp1582 USB2.0 device controller provides a high-speed interface for data exchange with a PC. 15..20 Mbytes/sec data throughput can be achieved. Bulk, Interrupt and isochronous transfers are supported. The D.Module2.BIOS greatly simplifies USB communications by providing a predefined interface with up to four user-definable endpoints. The DSP accesses the USB controller with CPU or DMA data transfers. An 8 Kbyte Fifo buffers incoming and outgoing data. In user-defined configurations up to 14 endpoints (7IN, 7OUT) can be used.

UART

A dual-channel UART with RS232 and RS422/485 line interface provides additional communication paths, supporting up to 230 Kbaud on RS232 and 3 Mbaud on RS422/485. The UART features 64 bytes transmit and receive Fifos for efficient block transfers and Xon/Xoff or RTS/CTS auto-flow-control. Data transfers can be accomplished by CPU (polling or interrupts) and DMA. The DModule2.BIOS provides configuration and data transfer functions.

I²C

The I²C interface can be used to control and configure peripherals like Audio Codecs, Image Sensors, and the analogue front-ends of data acquisition boards. It is also usable to expand the system with additional GPIO signals and attach temperature monitors.

PRGIO

16 bit-programmable I/Os are available on the DM642 module: 8 GPIO signals directly connected to the DSP, and 8 implemented in the Board Logic. Advanced features like interrupt on change are available. In OEM systems, the eight signals from the board logic can be reprogrammed to custom interfaces, e.g. PWM output.

POWER SUPPLY

The D.Module2.DM642 operates from a 3.3V single supply. All other required voltages (core voltage, RS232 driver supply, , etc.) are generated on-board by high-efficiency switch-mode converters and charge-pumps. The power supply is controlled by a supervisor chip, which guarantees a proper hardware reset on power-on, power-off, and brown-out conditions.

WATCHDOG

Stand-alone systems typically require methods for automatic recovery from system faults. One of these methods is activating the watchdog circuit. It will reset and reboot the system if the DSP program crashes and fails to trigger the watchdog periodically. The watchdog can be enabled (but not disabled) by software, or permanently by closing a solder link.

SYNCHRONOUS SERIAL PORTS

These ports, called McBSP on the D.Module2.DM642, provide a high-speed serial interface for A/D and D/A converters and Audio Codecs. The high transfer speed up to 150 Mbits/sec also make them usable as data links to FPGAs or other DSPs Besides the standard mode, the McBSPs can also operate as SPI master or slave interface.

The McBSPs share pins with the Video Ports: McBSP0 shares pins VP0, McBSP1 shares pins with VP1,

Note: The TMS320DM642 McASP0 signals are not available on the D.Module2.DM642

VIDEO PORTS

The three video ports with built-in capture and display buffers are ideally suited to connect image sensors, video encoders / decoders, and high-speed data converters. All ports support raw and BT.656 mode, VP2 also supports Y/C mode. VP0 and VP1 share pins with the McBSPs

BOARD CONFIGURATION

D.Module2 boards use a jumperless design, all board settings are software-configurable in the Board Configuration Register. The configuration can be set by the user program, or – preferably – stored in the Module Configuration File. At system start-up the Module configuration File is read and DSP clock, bus clock, and other options are configured accordingly.

The Board Configuration Register also provides multiplexers to route internal or external interrupt events to the DSP, and control and status registers for all on-board peripherals.

ETHERNET

The D.Module2.DM642 provides a 100Base-Tx / 10Base-T Ethernet interface, using the DM642 built-in MAC and an on-board PHY and magnetics. A highly optimized TCP/IP stack, tailored for DSP systems, is available from D.SignT too. Ethernet opens the door to remote control and maintenance, database-connectivity for biometric applications, Video-over-IP surveillance systems and many more new markets.

HPI / PCI

The HPI and PCI signals of the TMS320DM642 processor are not available on the D.Module2.DM642

D.MODULE2.BIOS

The BIOS is a set of API functions, permanently stored in the Flash Memory. These functions are copied to SDRAM at system start-up and are available to all user programs. BIOS functions cover initialization, configuration, and data transfer functions for the on-board peripherals. The reason to store these functions permanently in the Flash Memory, rather than providing them as a library, is the close coupling between low-level API functions and hardware: Should one of the module's peripherals need to be substituted during product lifetime, the BIOS will be adapted to the new hardware and the application program will continue to work without any changes.

USB functions

- open, close
- configure endpoints
- status change callback
- custom string descriptor table

- interrupt handler
- blockwrite, blockread
- low-level functions for user-defined interfaces

UART functions

- open, close
- configure
- write, blockwrite, write string
- read, blockread, read string

Flash Memory Functions

- open, get architecture information
- sector erase
- write, write block
- read, read block
- write Intel-Hex file

Board Functions

- initialize
- bootload
- get hardware and software revision
- DSP configuration and clocking
- external bus configuration and clocking
- delay
- watchdog enable and trigger
- interrupt and GPIO mapping
- read and clear multiplexed interrupts

SETUP AND RECOVERY PROGRAM

Also permanently stored in the Flash Memory are the Setup and Recovery utility programs. The Setup program communicates via RS232 or USB. It allows to upload Intel-Hex program and data files to the Flash Memory, upload a Module Configuration File, load and execute programs from Flash, and provides some basic debugging functions like reading and writing memory and memory-mapped peripherals. Setup is intended for field maintenance: Service technicians can upload program updates without direct access to the DSP hardware, and execute diagnostics and calibration programs stored in the Flash Memory.

The Recovery utility is stored in a hardware write protected Flash sector. Should the Flash be erased or overwritten accidentally, this program can be used to re-install the corrupted programs. Recovery uses a RS232 connection, even severe problems can be fixed in-field without special emulator programming equipment.

Setup is invoked during a module reset by pulling the SETUP_N input low, or at any time from within an application program by calling the BIOS bootload function: DM2_bootload (0x8000). Recovery is invoked at module reset by pulling both SETUP_N and IN1_N inputs low.

MEMORY MAP

Address	Memory	Location	Width	Description
0x0000.0000 .. 0x0000.01FF	IVT	internal		interrupt vector table
0x0000.0200 .. 0x0000.03FF	BIOS	internal		hardware initialization and bootloader code
0x0000.0400 .. 0x0001.FFFF	L2RAM	internal		127 Kbytes direct mapped L2RAM
0x0002.0000 .. 0x0003.0000	L2RAM	internal		64 Kbytes direct mapped L2RAM or L2-cache
0x0003.0000 .. 0x0003.7FFF	L2RAM	internal		32 Kbytes direct mapped L2RAM or L2-cache
0x0003.8000 .. 0x0003.FFFF	L2RAM	internal		32 Kbytes direct mapped L2RAM or L2-cache
0x0180.0000 .. 0x0200.0033		internal		DM642 on-chip peripheral control registers
0x8000.0000 .. 0x8000.3FFF	BIOS	CE0	64 bit	BIOS functions
0x8000.4000 .. 0x83FF.FFFF	SDRAM	CE0	64 bit	63.98 Mbytes free SDRAM
0x9000.0000 .. 0x900F.FFFF	FLASH	CE1	8 bit	8 Mbytes Flash Memory in 16 banks, 512 Kbytes each
0x9010.0000 .. 0x9010.0167	USB	CE1	16 bit	USB Controller
0x9014.0000 .. 0x9014.0003	USB	CE1	16 bit	USB Controller
0x9018.0000 .. 0x9018.000F	UART	CE1	8 bit	UART 0
0x9018.0010 .. 0x9018.001F	UART	CE1	8 bit	UART 1
0x901C.0000 .. 0x901C.003F	BOARD	CE1	8 bit	Board Configuration Registers
0xA000.0000 .. 0xAFFF.FFFF	CS0	CE2	32 bit	External Bus Interface CS0
0xB000.0000 .. 0xBFFF.FFFF	CS1	CE3	32 bit	External Bus Interface CS1

BOARD CONFIGURATION REGISTER

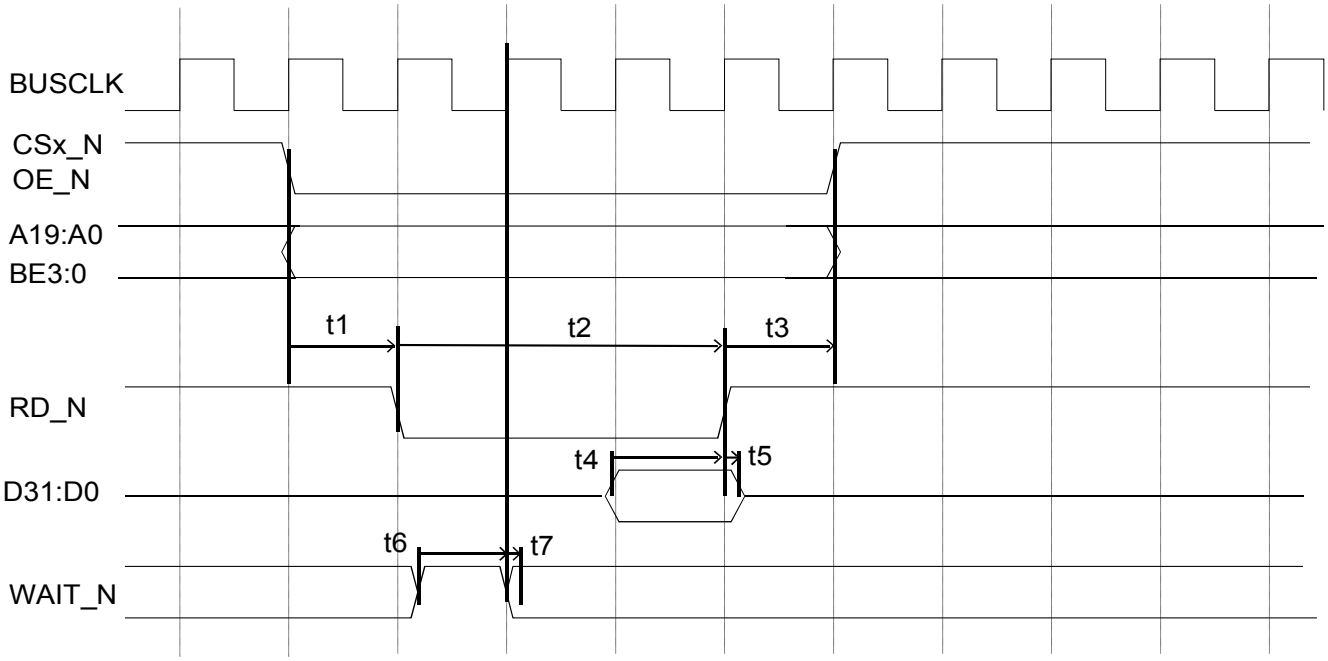
Register	D7	D6	D5	D4	D3	D2	D1	D0
USBCTRL	USBRES	-	-	-	-	INTSTAT	EOT_WR	EOT_RD
UARTCTRL	UARTRES	-	-	-	-	-	DRVEN_1	DRVEN_0
BUSCTRL	RESOUT	-	-	-	-	RDREG	FLYBY	SYYNC
WDOGCTRL	-	-	-	-	-	-	ENABLE	TRIGGER
DSPCTRL	DSPRES	CONFIG	ENDIAN	MACEN	DSPCLK		BUSCLK	
SETUPSTAT	-	-	-	-	-	SETUP	IN1	IN0
FLASHCTRL	-	-	-	-	A22	A21	A20	A19
INTMUXLO	INT5_SOURCE				INT4_SOURCE			
INTMUXHI	INT7_SOURCE				INT6_SOURCE			
GPIOMUXLO	GPIO1				GPIO0			
GPIOMUXHI	GPIO3				GPIO2			
MUXINTEN	UART1	UART0	PHY	CPLD	USB	-	-	-
MUXINTSRC	UART1	UART0	PHY	CPLD	USB	-	-	-
ETHCTRL	PHYRES	-	-	-	-	-	INTSTAT	LEDSTAT
PRGIODAT	DAT_IO7	DAT_IO6	DAT_IO5	DAT_IO4	DAT_IO3	DAT_IO2	DAT_IO1	DAT_IO0
PRGIODIR	DIR_IO7	DIR_IO6	DIR_IO5	DIR_IO4	DIR_IO3	DIR_IO2	DIR_IO1	DIR_IO0

SPECIFICATIONS

DSP	Texas Instruments TMS320DM642, fixed-point, up to 5760 million instructions per second 8/16/32/64-bit native data type support configurable core clock: 480, 600, or 720 MHz
Memory	256 Kbyte DSP-internal direct mapped or level-2 cache DSP-internal 16 Kbyte level-1 data cache, 16 Kbyte level-1 program cache 64 Mbytes SDRAM, operating at up to 133 MHz, 64 bits wide, 1Gbyte/sec throughput 8 Mbytes non-volatile Flash Memory, sector architecture , 8 bits wide
USB	Philps isp1582 USB2.0 peripheral controller, supports USB 1.1 and USB 2.0 up to 14 endpoints, 8 Kbyte shared FIFO, DMA support
UART	16C752 dual-channel UART, RS232 and RS422/485 line interface max. 230.4 Kbaud RS232, 3 Mbaud RS422/485, 64 bytes transmit and receive Fifos, DMA support, Auto-flow-control (Xon/Xoff, RTS/CTS)
Ethernet	100Base-Tx and 1Base-T, MAC built-in in DSP, on-board PHY and magnetics
I²C	built-in in DSP, supports up to 400 Kbits/sec, configurable as master or slave
Timer	built-in in DSP, two Timers with external inputs and outputs, 32 bit wide, internal or external clocking, a third 32 bit wide timer is available with internal clocking only
External Bus Interface	32 bit wide data bus, 20 address lines, 12 control signals supports synchronous and asynchronous operation, programmable and external wait states up to 533 Mbytes/sec throughput in synchronous mode configurable bus clock: 83, 100, 125, or 133 Mhz 3 external interrupt inputs, also using as DMA trigger
Sync. Serial Ports	2 McBSPs, independent receive and transmit channels, standard, TDM, and SPI mode data rate up to 150 Mbit/sec Note: McBSP0 shares pins with Video Port VP0, McBSP1 with VP1
Video Ports	3, with built-in capture / display buffers, up to 80 MHz clock VP0: 12 bit wide, supports raw and BT.656 format Note: shares pins with McBSP0 VP1: 10 bit wide, supports raw and BT.656 format Note: shares pins with McBSP0 VP2: 20 bit wide, supports raw, Y/C, and BT.656 format
Watchdog	enabled by software or hardware, timeout: 1 second
Emulation	standard 14-pin header, compatible with all JTAG inc-circuit emulators for TMS320C64x™ devices
Supply Voltage VCC	3.3 V ± 5%
Power Consumption	TBD
Operating Temperature	0 .. +70 °C
Logic Levels	LVTTL, High-Level min. 2V, max. 3.5V, Low Level min. -0.2V, max. 0.8V output drive: external bus interface: ± 24mA, all others ± 8mA
Size	86.8 x 58.4 mm, overall height: 19.5mm (can be reduced to 15.4 mm if JTAG connector is removed)
Weight	36g
Connectors	COM, EXP, BUS1 and BUS2 : Molex 71436-2164 Emulator: standard 14-pin header
industrial grade version	operating temperature -40 .. +85°C DSP core clock 480 or 600 MHz external bus and SDRAM clock 83.3 or 100 MHz

TIMINGS

external bus asynchronous read

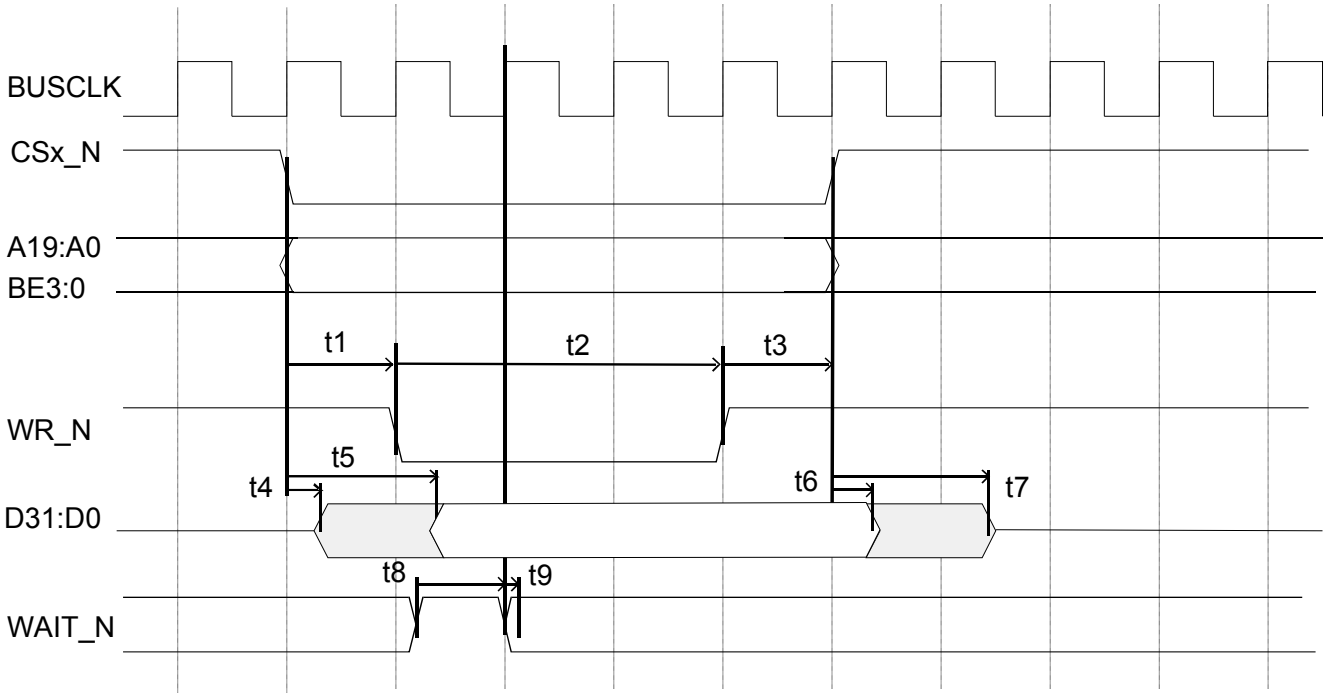


Timing	min	max	Description
t1	programmed SETUP cycles *1)		address and control signals setup before read strobe activated
t2	programmed STROBE cycles *1)		read strobe width
t3	programmed HOLD cycles *1)		address and control signals hold after read strobe deactivated
t4	10.4 ns		data valid before read strobe deactivated
t5	0 ns		data valid after read strobe deactivated
t6	5.3 ns 8 ns ind. grade		WAIT_N high before BUSCLK rising edge *2)
t7	1.5 ns		WAIT_N high after BUSCLK rising edge *2)

*1) setup, hold, and strobe cycles are programmed in the EMIF control registers. The timing is based on BUSCLK, which is programmable to 83.3 MHz (12 ns cycle time), 100 MHz (10 ns cycle time), 125 MHz (8 ns cycle time) or 133 MHz (7.5 ns cycle time)

*2) WAIT_N is sampled two cycles before the end of the programmed strobe period. If WAIT_N is found low at this time, the current bus cycle is extended until WIAT_N is sampled high. Two cycles after WAIT_N is high, the strobe cycle ends.

external bus asynchronous write

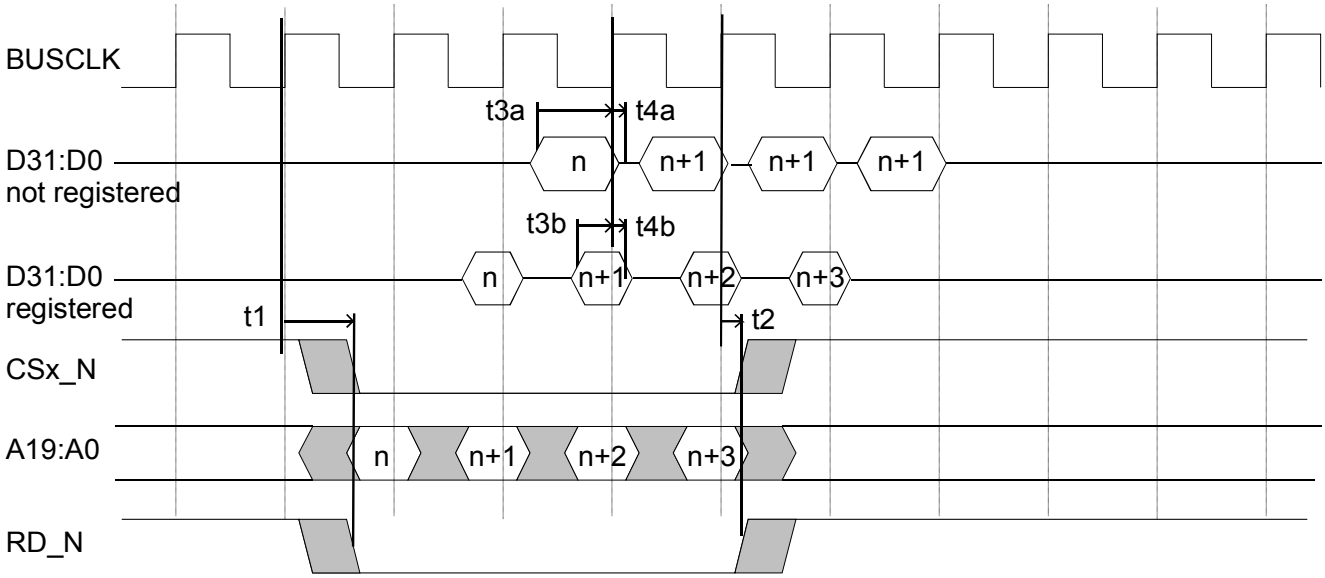


Timing	min	max	Description
t1	programmed SETUP cycles *1)		address and control signals setup before write strobe activated
t2	programmed STROBE cycles *1)		write strobe width
t3	programmed HOLD cycles *1)		address and control signals hold after write strobe deactivated
t4	2.4 ns		bus driver active after control signals valid
t5		6.9 ns 9.6ns ind. grade	data valid after control signals valid
t6	2.4 ns		data hold after control signals invalid
t7		6.9 ns 9.6ns ind. grade	bus driver disabled after control signals invalid
t8	5.3 ns 8 ns ind. grade		WAIT_N high before BUSCLK rising edge *2)
t9	1.5 ns		WAIT_N high after BUSCLK rising edge *2)

*1) setup, hold, and strobe cycles are programmed in the EMIF control registers. The timing is based on BUSCLK, which is programmable to 83.3 MHz (12 ns cycle time), 100 MHz (10 ns cycle time), 125 MHz (8 ns cycle time) or 133 MHz (7.5 ns cycle time)

*2) WAIT_N is sampled two cycles before the end of the programmed strobe period. If WAIT_N is found low at this time, the current bus cycle is extended until WIAT_N is sampled high. Two cycles after WAIT_N is high, the strobe cycle ends.

external bus synchronous read

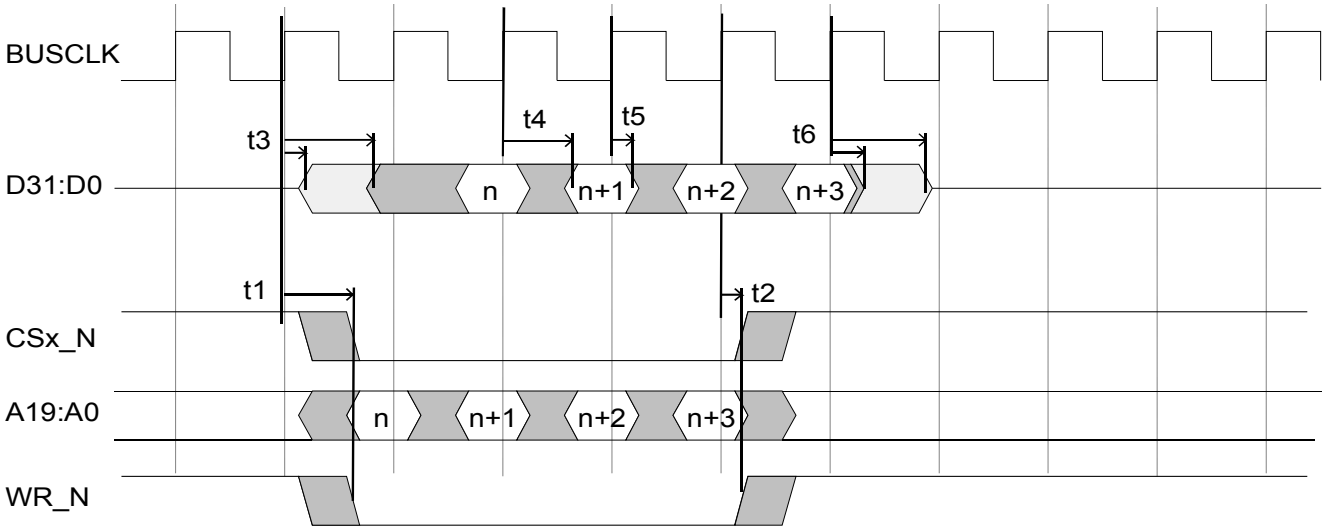


Timing	min	max	Description
t1		4.9 ns	BUSCLK rising edge to address and control signals valid
t2	1.4 ns		address and control signals hold after BUSCLK rising edge
t3a	5.9 ns 7 ns ind. grade		unregistered reads: data setup to BUSCLK rising edge
t3b	1.7ns		registered reads: data setup to BUSCLK rising edge
t4a	0 ns		unregistered reads: data hold after BUSCLK rising edge
t4b	0.7ns		registered reads: data hold after BUSCLK rising edge

BUSCLK, is programmable to 83.3 MHz (12 ns cycle time), 100 MHz (10 ns cycle time), 125 MHz (8 ns cycle time) or 133 MHz (7.5 ns cycle time)

The synchronous interface is configurable to registered or unregistered reads. Registered reads simplify the interface because of relaxed data setup timing, unregistered reads however offer one more pipeline cycle between read command and data.

external bus synchronous write



Timing	min	max	Description
t1		4.9 ns	BUSCLK rising edge to address and control signals valid
t2	1.4 ns		address and control signals hold after BUSCLK rising edge
t3	2 ns	6.6 ns 8 ns ind. grade	bus driver active after BUSCLK rising edge
t4		4.9 ns	BUSCLK rising edge to data valid
t5	1.4 ns		data hold from BUSCLK rising edge
t6	2 ns	7.3 ns 8.5 ns ind. grade	bus driver disabled after BUSCLK rising edge

BUSCLK, is programmable to 83.3 MHz (12 ns cycle time), 100 MHz (10 ns cycle time), 125 MHz (8 ns cycle time) or 133 MHz (7.5 ns cycle time)

Video Ports, McBSP Timings

these signals are directly connected to the DSP. Please refer to the Texas Instruments TMS320DM642 data sheet for detailed information

PINOUT AND SIGNAL DESCRIPTION

COM Connector

Signal	Pin	Type	Description
GND_IN	1,2,3,4	PWR	Power Supply Input, 0V
VCC_IN	5,6,7,8	PWR	Power Supply Input, 3.3V
SETUP_N	9	I	Setup Input, active low, internal 10K pull-up, start Setup-Utility if found low at reset
IN0_N	10	I	active low, internal 10K pull-up, start Recovery-Utility if SETUP_N and IN0_N are found low at reset
IN1_N	12	I	active low, internal 10K pull-up, reserved for configuration
RESIN_N	11	I	Reset Input, active low, internal 10K pull-up
USB_VCC	13	I	USB Power, supplied by Host or Hub, used to detect USB cable
USB_GND	15	I	USB power and reference signal ground
USB_D+	14	IO DIF	USB data, non-inverted signal
USB_D-	16	IO DIF	USB data, inverted signal
CTS0	19	I	UART0, RS232 CTS (if RS422: RDX0-)
RTS0	20	O	UART0, RS232 RTS (if RS422: TXD0-)
RXD0	21	I	UART0, RS232 data input (if RS422: RXD0+)
TXD0	22	O	UART0, RS232 data input (if RS422: TXD0+)
RXD1-	25	I DIF	UART1, RS422 inverted data input (if RS232: CTS1)
RXD1+	27	I DIF	UART1, RS422 non-inverted data input (if RS232: RXD1)
TXD1-	26	O DIF	UART1, RS422 inverted data output (if RS232: RTS1)
TXD1+	28	O DIF	UART1, RS422 non-inverted data output (if RS232: TXD1)
ETH_GND	29, 30		100Base-Tx Ethernet ground
ETH_RX+	31	I DIF	100Base-Tx Ethernet non-inverted data input
ETH_RX-	33	I DIF	100Base-Tx Ethernet inverted data input
ETH_TX+	32	O DIF	100Base-Tx Ethernet non-inverted data output
ETH_TX-	34	O DIF	100Base-Tx Ethernet inverted data output
SCL	37	IOZ	I²C Bus Clock, internal 4K7 pull-up
SDA	38	IOZ	I²C Bus Data, internal 4K7 pull-up
PRGIO0..7	43,45,46,48, 49,50,51,53	IOZ	programmable I/O signal from Board Logic
PRGIIO8..15	54,56,57,58, 59,61,62,64	IOZ	GPIO3, GPIO9..GPIO15 from DSP
SGND	17,18,23,24, 35,36,40,41, 44,47,52,55, 60,63		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power, DIF – differential signal

EXP Connector

Signal	Pin	Type	Description
VP2D0..VP2D19	2,3,4,5, 7,8,10,11, 12,13,15,16, 18,19,20,21, 23,24,26,27	IO	Video Port 2 data
VP2CTL0 VP2CTL1 VP2CTL2	28 29 31	IO	Video Port 2 programmable control signals
VP2CLK0 VP2CLK1	32 34	IO	Video Port 2 programmable clocks
VP1D0 VP1D1 VP1D2 VP1D3 VP1D4 VP1D5 VP1D6 VP1D7 VP1D8 VP1D9	35 36 BUS2-58 * BUS2-59 * BUS2-57 * 37 BUS2-54 * BUS2-56 * BUS2-55 * 39	IO	Video Port 1 data
VP1CTL0 VP1CTL1 VP1CTL2	40 42 44	IO	Video Port 1 programmable control signals
VP1CLK0 VP1CLK1	43 45	IO	Video Port 1 programmable clocks
VP0D0 VP0D1 VP0D2 VP0D3 VP0D4 VP0D5 VP0D6 VP0D7 VP0D8 VP0D9 VP0D10 VP0D11	47 48 BUS2-51 * BUS2-52 * BUS2-49 * 50 BUS2-46 * BUS2-48 * BUS2-47 * 51 52 53	IO	Video Port 0 data
VP0CTL0 VP0CTL1 VP0CTL2	55 56 58	IO	Video Port 0 programmable control signals
VP0CLK0 VP0CLK1	59 60	IO	Video Port 0 programmable clocks
STCTL	63	I	Master Clock Input for VP0..2
VCTL	64	O	DAC Output for Genlock VCXO
SGND	1,6,9,14, 17,22,25,30, 33,38,41,46, 49,54,57,61, 62		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power

* multiplexed with McBSP peripheral

BUS 1 Connector

Signal	Pin	Type	Description
VCC_OUT	1, 2	PWR	Power Supply Output to Peripherals, +3.3V
GND_OUT	3, 4	PWR	Power Supply Output to Peripherals, 0V
AGND	59, 60	PWR	Analogue Power Supply to Peripherals, 0V
AVCC+	61, 62	PWR	Analogue Power Supply to Peripherals, positive voltage rail
AVCC-	63, 64	PWR	Analogue Power Supply to Peripherals, negative voltage rail
RESOUT_N	5	O	Reset Output to Peripherals, active low
BUSCLK	6	O	Bus Clock, use if external bus configured to synchronous operation
INT0_N, INT1_N, INT2_N	7, 9, 10	I	External Interrupt Inputs, active low, internal 1K pull-up
BE2_N, BE3_N	12, 14	O	Byte Enable for D16..D23 and D24..D31, active low
OE_N	13	O	Output Enable, active low, asserted during Read Cycles
RD_N	15	O	Read Strobe, active low
WR_N	17	O	Write Strobe, active low
WAIT_N	18	I	Wait State Request, active low, internal 1K pull-up
CS0_N	20	O	Chip Select 0, active low
CS1_N	22	O	Chip Select 1, active low
A0..A5	21,23,25,26, 28,29	O	Address Bus
A16..A19	30,31,33,34	O	Address Bus
D16..D31	36,37,38,39, 41,42,44,45, 46,47,49,50, 52,53,54,55	IOZ	Data Bus
GPIO0, GPIO1	57, 58	IOZ	General Purpose IO, or IORD_N, IOWR_N during FlyBy DMA Transfers
SGND	8,11,16,19, 24,27,32,35, 40,43,48,51, 56		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power

BUS 2 Connector

Signal	Pin	Type	Description
VCC_OUT	63, 64	PWR	Power Supply Output to Peripherals, +3.3V
GND_OUT	61, 62	PWR	Power Supply Output to Peripherals, 0V
AGND	5, 6	PWR	Analogue Power Supply to Peripherals, 0V
AVCC+	3, 4	PWR	Analogue Power Supply to Peripherals, positive voltage rail
AVCC-	1, 2	PWR	Analogue Power Supply to Peripherals, negative voltage rail
GPIO2, GPIO3	7, 8	IOZ	General Purpose IO
D0..D15	9,10,11,12, 14,15,16,17, 19,20,22,23, 24,25,27,28	IOZ	Data Bus
A6..A15	30,31,32,33, 35,36,38,39, 40,41	O	Address Bus
BE0_N, BE1_N	43, 44	O	Byte Enable for D0..D7 and D8..D15, active low
DATR0 / VP0D6	46	I	Sync Serial Port 0, data receiver, mux'ed with video port 0
CLKR0 / VP0D8	47	IO	Sync Serial Port 0, receive clock input or output, mux'ed with video port 0
FSR0 / VP0D7	48	IO	Sync Serial Port 0, receive frame sync input or output, mux'ed with video port 0
DATX0 / VP0D4	49	O	Sync Serial Port 0, data transmitter, mux'ed with video port 0
CLKX0 / VP0D2	51	IO	Sync Serial Port 0, transmit clock input or output, mux'ed with video port 0
FSX0 / VP0D3	52	IO	Sync Serial Port 0, transmit frame sync input or output, mux'ed with video port 0
DATR1 / VP1D6	54	I	Sync Serial Port 1, data receiver, mux'ed with video port 1
CLKR1 / VP1D8	55	IO	Sync Serial Port 1, receive clock input or output, mux'ed with video port 1
FSR1 / VP1D7	56	IO	Sync Serial Port 1, receive frame sync input or output, mux'ed with video port 1
DATX1 / VP1D4	57	O	Sync Serial Port 1, data transmitter, mux'ed with video port 1
CLKX1 / VP1D2	58	IO	Sync Serial Port 1, transmit clock input or output, mux'ed with video port 1
FSX1 / VP1D3	59	IO	Sync Serial Port 1, transmit frame sync input or output, mux'ed with video port 1
RESOUT_N	60	O	Reset Output to Peripherals, active low
SGND	13,18,21,26, 29,34,37,42, 45,50,53,		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power

BUS 1

Pin	Signal	Signal	Pin
1	VCC_OUT	VCC_OUT	2
3	GND_OUT	GND_OUT	4
5	RESOUT_N	BUSCLK	6
7	INT0_N	SGND	8
9	INT1_N	INT2_N	10
11	SGND	BE2_N	12
13	OE_N	BE3_N	14
15	RD_N	SGND	16
17	WR_N	WAIT_N	18
19	SGND	CS0_N	20
21	A0	CS1_N	22
23	A1	SGND	24
25	A2	A3	26
27	SGND	A4	28
29	A5	A16	30
31	A17	SGND	32
33	A18	A19	34
35	SGND	D16	36
37	D17	D18	38
39	D19	SGND	40
41	D20	D21	42
43	SGND	D22	44
45	D23	D24	46
47	D25	SGND	48
49	D26	D27	50
51	SGND	D28	52
53	D29	D30	54
55	D31	SGND	56
57	GPIO0	GPIO1	58
59	AGND	AGND	60
61	AVCC+	AVCC+	62
63	AVCC-	AVCC-	64

COM

Pin	Signal	Signal	Pin
1	GND_IN	GND_IN	2
3	GND_IN	GND_IN	4
5	VCC_IN	VCC_IN	6
7	VCC_IN	VCC_IN	8
9	SETUP_N	IN0_N	10
11	RESIN_N	IN1_N	12
13	USB_VCC	USB_D+	14
15	USB_GND	USB_D-	16
17	SGND	SGND	18
19	CTS_0	RTS_0	20
21	RXD_0	TXD_0	22
23	SGND	SGND	24
25	RXD_1-	TXD_1-	26
27	RXD_1+	TXD_1+	28
29	ETH_GND	ETH_GND	30
31	ETH_RX+	ETH_TX+	32
33	ETH_RX-	ETH_TX-	34
35	SGND	SGND	36
37	SCL	SDA	38
39	rsvd	SGND	40
41	SGND	rsvd (CLKIN)	42
43	PRGIO0	SGND	44
45	PRGIO1	PRGIO2	46
47	SGND	PRGIO3	48
49	PRGIO4	PRGIO5	50
51	PRGIO6	SGND	52
53	PRGIO7	PRGIO8	54
55	SGND	PRGIO9	56
57	PRGIO10	PRGIO11	58
59	PRGIO12	SGND	60
61	PRGIO13	PRGIO!4	62
63	SGND	PRGIO15	64

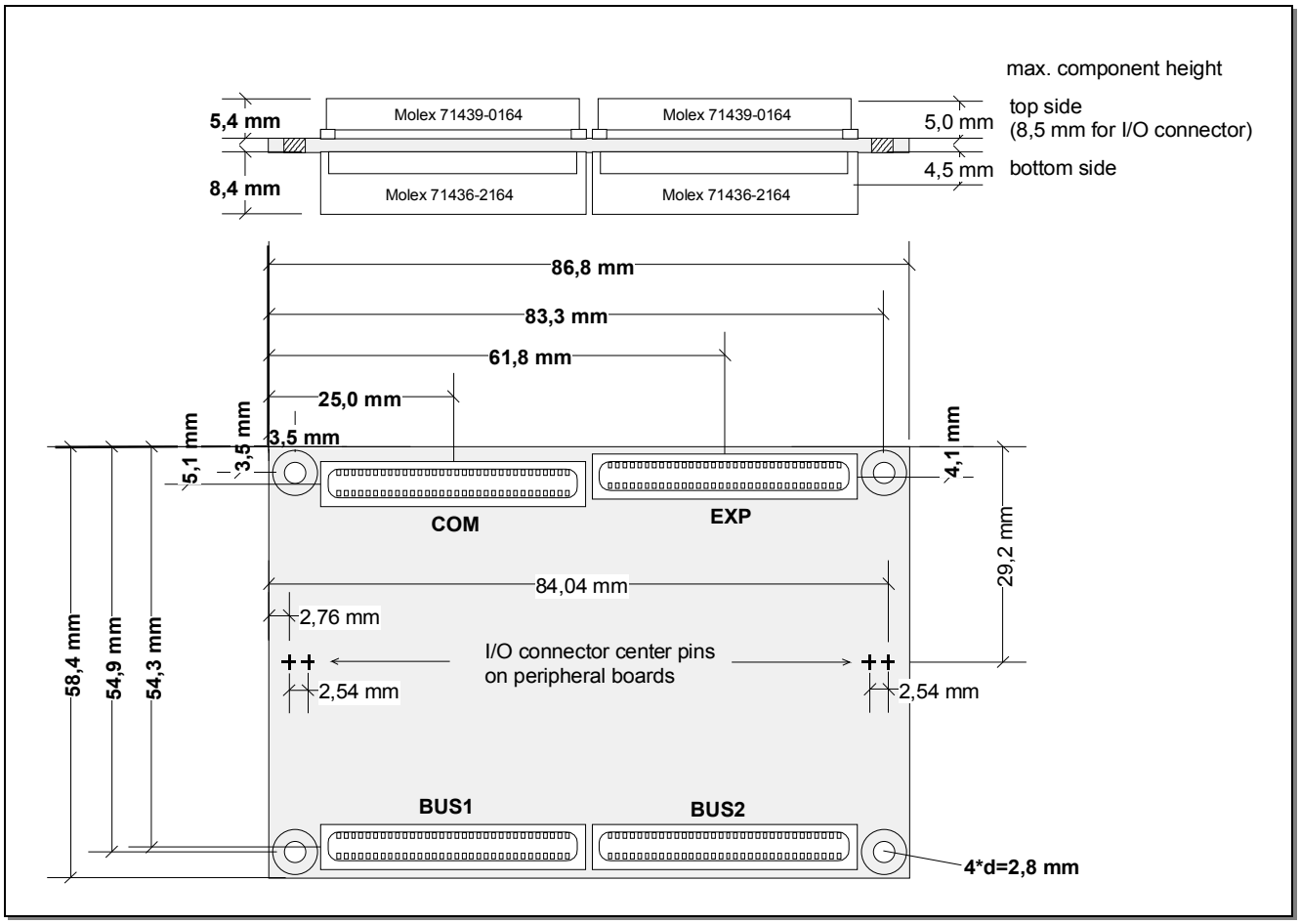
BUS 2

Pin	Signal	Signal	Pin
1	AVCC-	AVCC-	2
3	AVCC+	AVCC+	4
5	AGND	AGND	6
7	GPIO2	GPIO3	8
9	D0	D1	10
11	D2	D3	12
13	SGND	D4	14
15	D5	D6	16
17	D7	SGND	18
19	D8	D9	20
21	SGND	D10	22
23	D11	D12	24
25	D13	SGND	26
27	D14	D15	28
29	SGND	A6	30
31	A7	A8	32
33	A9	SGND	34
35	A10	A11	36
37	SGND	A12	38
39	A13	A14	40
41	A15	SGND	42
43	BE0_N	BE1_N	44
45	SGND	DATR0	46
47	CLKR0	FSR0	48
49	DATX0	SGND	50
51	CLKX0	FSX0	52
53	SGND	DATR1	54
55	CLKR1	FSR1	56
57	DATX1	CLKX1	58
59	FSX1	RESOUT_N	60
61	GND_OUT	GND_OUT	62
63	VCC_OUT	VCC_OUT	64

EXP

Pin	Signal	Signal	Pin
1	SGND	VP2D0	2
3	VP2D1	VP2D2	4
5	VP2D3	SGND	6
7	VP2D4	VP2D5	8
9	SGND	VP2D6	10
11	VP2D7	VP2D8	12
13	VP2D9	SGND	14
15	VP2D10	VP2D11	16
17	SGND	VP2D12	18
19	VP2D13	VP2D14	20
21	VP2D15	SGND	22
23	VP2D16	VP2D17	24
25	SGND	VP2D18	26
27	VP2D19	VP2CTL0	28
29	VP2CTL1	SGND	30
31	VP2CTL2	VP2CLK0	32
33	SGND	VP2CLK1	34
35	VP1D0	VP1D1	36
37	VP1D5	SGND	38
39	VP1D9	VP1CTL0	40
41	SGND	VP1CTL1	42
43	VP1CLK0	VP1CTL2	44
45	VP1CLK1	SGND	46
47	VP0D0	VP0D1	48
49	SGND	VP0D5	50
51	VP0D9	VP0D10	52
53	VP0D11	SGND	54
55	VP0CTL0	VP0CTL1	56
57	SGND	VP0CTL2	58
59	VP0CLK0	VP0CLK1	60
61	SGND	SGND	62
63	STCTL	VCTL	64

MECHANICAL DIMENSIONS



ORDERING INFORMATION

D.Module2.DM642	standard module
Options:	-I : industrial grade, max. 600 MHz DSP core clock, max. 100 MHz Bus and SDRAM clock OEM quantities (25++) only
DS.DM642	Development Support Package including support software, base board, cables, power supply, and documentation
DS.TCP/IP-DM642	TCP/IP Evaluation Package including D.SignT TCP/IP protocol library, sample programs for DSP and PC, documentation, and evaluation license
TMDSCCSALL-1	Texas Instruments Code Composer Studio code generation and debug tools
XDS560R	Spectrum Digital high-speed USB2.0 JTAG in-circuit emulator
XDS510USB_PLUS	Spectrum Digital high-speed USB2.0 JTAG in-circuit emulator
XDS510USB	Spectrum Digital USB JTAG in-circuit emulator
XDS510pp_plus	Spectrum Digital parallel port JTAG in-circuit emulator

Additional Options On Volume Purchase

For volume purchase D.SignT offers customer specific modifications of the hardware either to reduce costs through reduced functionality or to increase functionality to meet the customers application requirements. Extensive experience in custom designs and the powerful engineering tools of our development department bring your application and our DSP know how together for your solution. Please contact D.SignT directly.

Technical Support

Our products include free of charge technical support. You can reach the technical support by e-mail (support@dsignt.de) phone or fax.

Pricing

Please ask for our current price list and volume discounts.

Availability

Our standard D.Modules are available typically ex-stock.- For special modifications or non-standard D.Module2 please consult our sales department.

Warranty

All D.Module2 boards come with a 12 month warranty .